WHAT IS CLAIMED IS:

1. A multiple channel transistor comprising:

a silicon substrate;

a first gate oxide layer on the substrate;

a carrier confinement layer on the first gate oxide layer;

a silicon layer on the carrier confinement layer, the silicon layer and the carrier confinement layer having sidewalls;

a second gate oxide layer on the silicon layer;

a gate on the second gate oxide layer; and

source and drain regions in the substrate and on the silicon layer sidewalls and the carrier confinement layer sidewalls.

2. The transistor of claim 1,wherein the carrier confinement layer is between about 50 Å to about 200 Å thick.

3. The transistor of claim 2, wherein the carrier confinement layer consists of SiGe.

4. The transistor of claim 2, wherein the carrier confinement layer consists of doped Ge.

5. The transistor of claim 2, wherein the carrier confinement layer consists of a high dielectric constant semiconductor.

6. The transistor of claim 1, wherein the silicon layer is a strained silicon layer.

7. The transistor of claim 1, wherein the substrate includes a strained silicon layer.

8. The transistor of claim 1, wherein the carrier confinement layer is a hole confinement layer.

9. The transistor of claim 1, wherein the carrier confinement layer is an electron confinement layer.

10. A multi-channel transistor, comprising:

a first channel and a second channel; and

a carrier confinement layer between the first and second channels to confine carriers produced by hot carrier effects in the first channel that switch on the second channel.

11. The transistor of claim 10, wherein the charge confinement layer is a high dielectric constant semiconductor.

12. The transistor of claim 11, wherein at least one of the first and second channels comprises a strained silicon layer.

13. The transistor of claim 12, wherein the charge confinement layer comprises at least one of Ge or SiGe.

14. The transistor of claim 13, further comprising a substrate in which the second channel is formed, and a first gate oxide layer on the substrate, the charge confinement layer being on the first gate oxide layer.

15. The transistor of claim 14, further comprising a silicon layer on the charge confinement layer, the silicon layer being a strained silicon layer and the first channel being formed on the silicon layer.

16. The transistor of claim 15, further comprising a second gate oxide layer on the silicon layer, and a gate on the second gate oxide layer.

17. The transistor of claim 16, further comprising source and drain regions in the substrate and on the carrier confinement layer and the silicon layer.

18. The transistor of claim 17, wherein the charge confinement layer is between about 50 to about 200 Å thick.